GLS85LE1xxxT

Industrial Temp **NVMe NANDrive™** PX Series

Advance Factsheet 00.100
February 2024

Features

- **Industry Standard PCIe Host Interface**
  - PCIe Gen3x4
  - PCI Express Base Revision 3.1 compliant
  - NVMe 1.4c compliant
- **Performance**
  - Sequential data read: Up to 2,380 MB/s
  - Sequential data write: Up to 665 MB/s (measured using 128KB transfer size)
- **Power Management**
  - 3 power supplies (PWR_1/2/3 = 3.3V/1.8V/0.9V)
  - Autonomous power state transition (APST)
  - Active state power management (ASPM)
  - Supports L1.2 link state
- **Power Consumption**
  - Active mode (typical):
    512GB: 2,755 mW
    256GB: 2,650 mW
    128GB: 1,866 mW
    64GB: 1,390 mW
  - Idle/Slumber mode (typical): 108 mW/57 mW
  - Sleep mode (typical): 3.8 mW (512GB)
- **Data Protection**
  - End-to-end data path protection
  - AES-256 encryption engine
  - Hardware Crypto Erase (HCE)
  - Secure erase / Data sanitization
  - Host Controlled Thermal Management (HCTM)
  - Thermal throttling
- **Supports up to 4 Namespaces**
- **Boot Partition**
- **Replay Protected Memory Block (RPMB)**
- **Host Memory Buffer (HMB)**
- **Volatile Write Cache (VWC)**
- **Field Firmware Update (FFU)**
- **Supports SMART and TRIM Commands**
- **Power Loss Notification**
- **Command Queuing**
  - 1 Admin queue and 8 IO queues supporting up to 128 commands per queue
- **Dynamic and Static Wear-Leveling**
- **Bad Block Management**
- **Built-in ECC**
  - Uses advanced LDPC bit error detection and correction optimized for 3D NAND
- **NAND Configuration**
  - 3 bits per cell (TLC)
- **Endurance**
  - P/E cycles: 5K, TBW (512GB): 1,350
- **Operating Temperature Range**
  - Industrial: -40°C to 95°C (Tc)
- **BGA Package**
  - 16.0 mm x 20.0 mm x 1.40 mm, 291-ball, 0.8 mm ball pitch, LTE (LFBGA)
  - 16.0 mm x 20.0 mm x 1.85 mm, 291-ball, 0.8 mm ball pitch, F1TE (FBGA)
- **All Devices are RoHS Compliant**

Notes: 1. User capacity: 1GB = 1 billion bytes
2. PCIe = Peripheral Component Interconnect Express
3. NVMe = Non-Volatile Memory Express
4. P/E cycles = NAND Program/Erase cycles
5. TBW = TeraBytes Written
6. Tc = Case surface temperature

Product Description

The GLS85LE1xxxT Industrial Temp NVMe NANDrive™ PX Series (referred to as "NVMe NANDrive" in this datasheet) are high-performance, high-reliability solid state drives (SSDs). They combine an advanced Greenliant NAND controller with 64, 128, 256 or 512 GBytes of NAND flash memory in a multi-chip package.

The integrated NAND flash controller with built-in advanced NAND management firmware communicates with the host through the standard PCIe interface. It does not require any additional or proprietary software such as the Flash File System (FFS) and Memory Technology Driver (MTD). The firmware effectively optimizes the use of NAND flash memory's program/erase (P/E) cycles and minimizes write amplification.

NVMe NANDrive's advanced NAND management technology improves endurance, enhances data security and helps prevent data corruption during unexpected power failure events. This innovative technology combines robust NAND controller hardware error correction capabilities with advanced wear-leveling algorithms and bad block management to improve data reliability and significantly extend the life of the product. NVMe NANDrive is ideal for high-reliability industrial and networking systems which need low latency and fast performance.

1.0 GENERAL DESCRIPTION

Each NVMe NANDrive module integrates an NVMe PCIe NAND flash memory controller with discrete NAND flash die in a BGA package. Refer to Figure 2-1 for the NVMe NANDrive block diagram.

1.1 Optimized NVMe NANDrive

The heart of NVMe NANDrive is the NVMe PCIe NAND flash memory controller, which translates standard PCIe signals into flash media data and control signals. The following components contribute to NVMe NANDrive's operation.

1.1.1 Microcontroller Unit (MCU)

The MCU translates PCIe / NVMe commands into data and control signals required for flash media operation.

1.1.2 Internal Direct Memory Access (DMA)

NVMe NANDrive uses internal DMA allowing instant data transfer from/to buffer to/from flash media. This implementation eliminates microcontroller overhead associated with the traditional, firmware-based approach, thereby increasing the data transfer rate.

1.1.3 Power Management Unit (PMU)

The PMU controls the power consumption of NVMe NANDrive. The PMU dramatically reduces the power consumption of NVMe NANDrive by putting the part of the circuitry that is not in operation into sleep mode.

The Flash File System handles inadvertent power interrupts and has auto-recovery capability to ensure NVMe NANDrive firmware integrity.

1.1.4 Embedded Flash File System

The embedded flash file system is an integral part of NVMe NANDrive. It contains MCU firmware that performs the following tasks:

1. Translates host side signals into flash media writes and reads
2. Provides flash media wear leveling to spread the flash writes across all memory address space to increase the longevity of flash media
3. Keeps track of data file structures

1.1.5 Error Checking and Correction (ECC)

The ECC technology uses advanced LDPC algorithms to detect and correct errors, ensuring data integrity and extending the SSD lifespan.

1.1.6 Multi-tasking Interface

The multi-tasking interface enables concurrent Read, Program and Erase operations to multiple NAND flash media.

1.2 SMT Reflow Consideration

The NVMe NANDrive family utilizes standard NAND flash for data storage. Because the high temperature in a surface-mount reflow soldering process may alter the content on NAND flash, it is recommended to program the NVMe NANDrive after the reflow process.

1.3 Advanced NAND Management

NVMe NANDrive's controller uses advanced wear-leveling algorithms to substantially increase the longevity of NAND flash media. Wear caused by data writes is evenly distributed in all or select blocks in the device that prevents "hot spots" in locations that are programmed and erased extensively. This effective wear-leveling technique results in optimized device endurance, enhanced data retention and higher reliability required by long-life applications.

1.4 Advanced Data Security

Advanced data security measures include end-to-end data path protection, data sanitization (Secure Erase) support and Hardware cryptographic erase. Secure Erase is an effective method to quickly wipe all data from a PCIe-based SSD using the NVMe protocol (Format NVM). NVMe NANDrive's controller supports industrial standard AES-256 encryption to protect sensitive user data. Hardware Cryptographic Erase resets the cryptographic keys of the NVMe NANDrive SSD, making all encrypted user data useless.

2.0 FUNCTIONAL BLOCKS

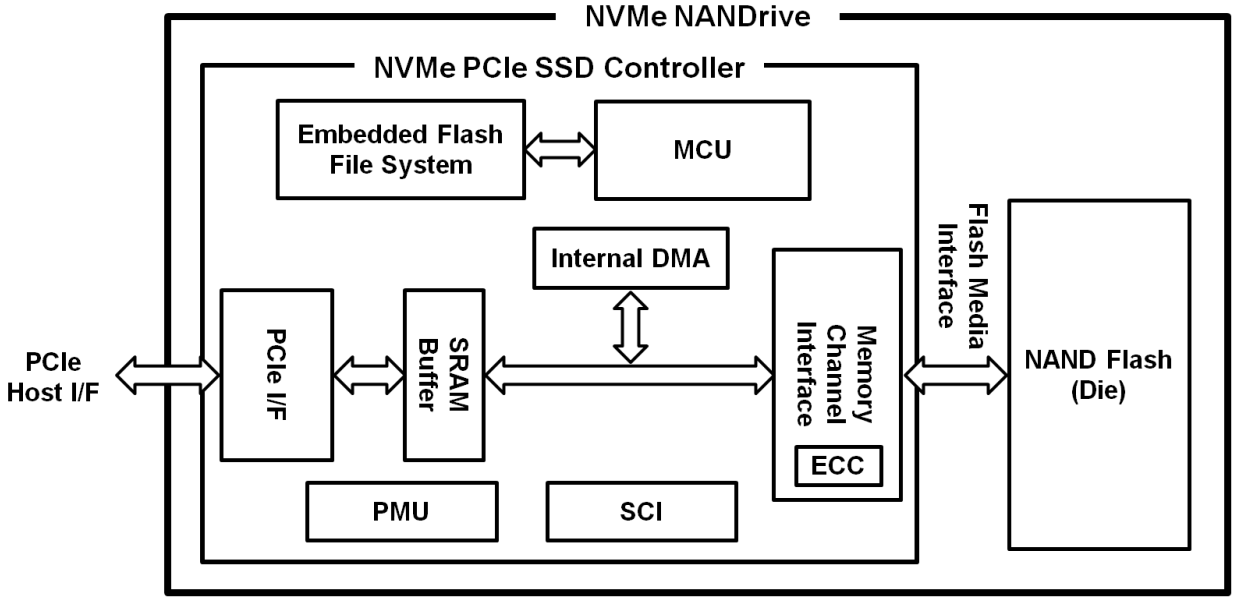
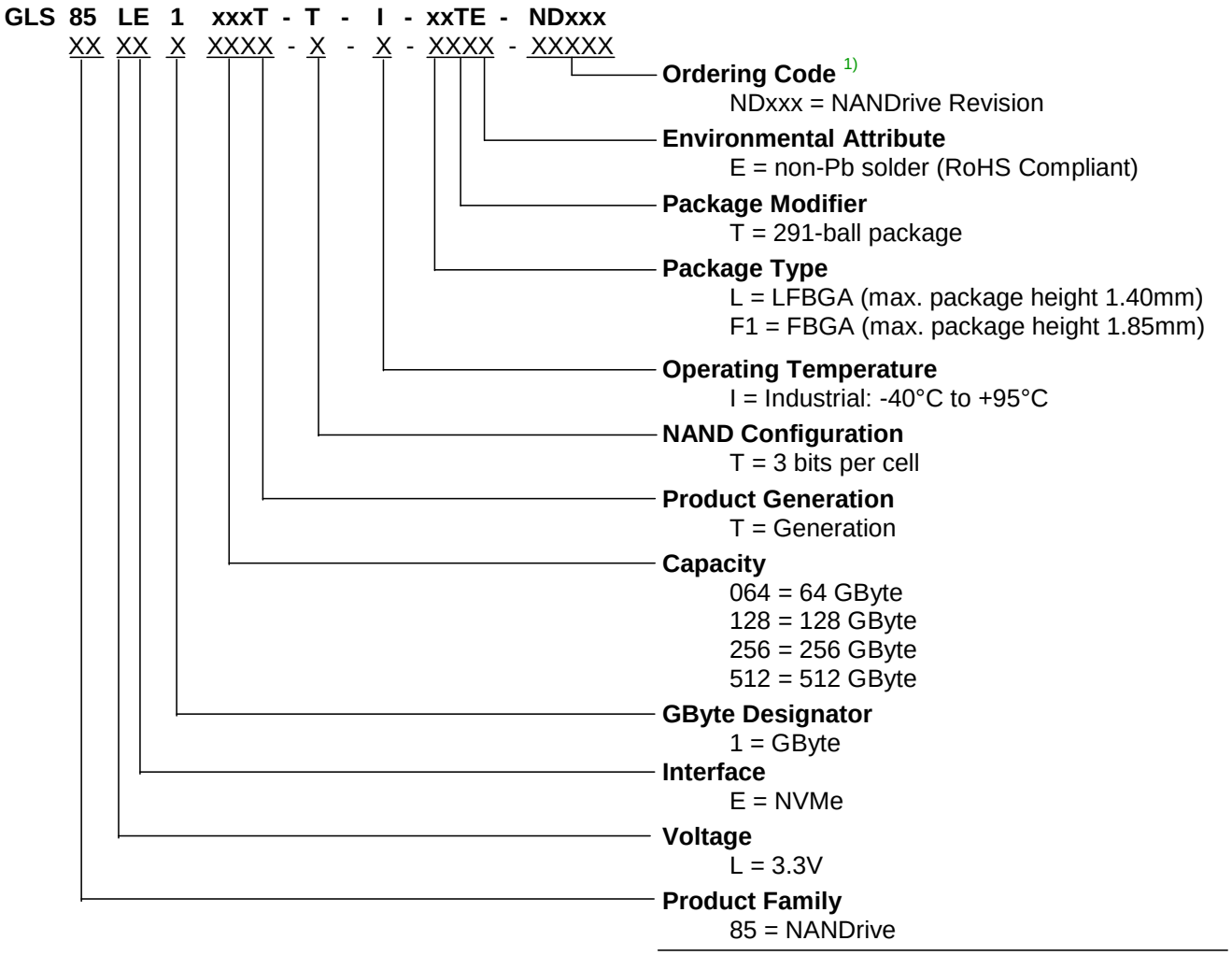


Figure 2-1: NVMe NANDrive Block Diagram

3.0 Product Ordering Information



1) Note that the top side marking on the package typically does not include ordering codes (e.g. NDxxx), unless it is a special custom specification (C-SPEC) required by the end-customer to be marked on the device.

Valid Combinations

Valid product combinations are those that are in the mass production or will be in the mass production. Consult your Greenliant sales representative to confirm availability of the valid combinations and to determine availability of new product combinations.

Table 3-1: NVMe NANDrive Product Valid Ordering Numbers

Capacity	Operating Temperature	Part Number	Package
64GB	Industrial (Tc = -40°C to 95°C)	GLS85LE1064T-T-I-LTE-ND300	LTE, 16x20x1.40mm
128GB	Industrial (Tc = -40°C to 95°C)	GLS85LE1128T-T-I-LTE-ND300	LTE, 16x20x1.40mm
256GB	Industrial (Tc = -40°C to 95°C)	GLS85LE1256T-T-I-LTE-ND300	LTE, 16x20x1.40mm
512GB	Industrial (Tc = -40°C to 95°C)	GLS85LE1512T-T-I-F1TE-ND300	F1TE, 16x20x1.85mm

3.1 Package Diagrams

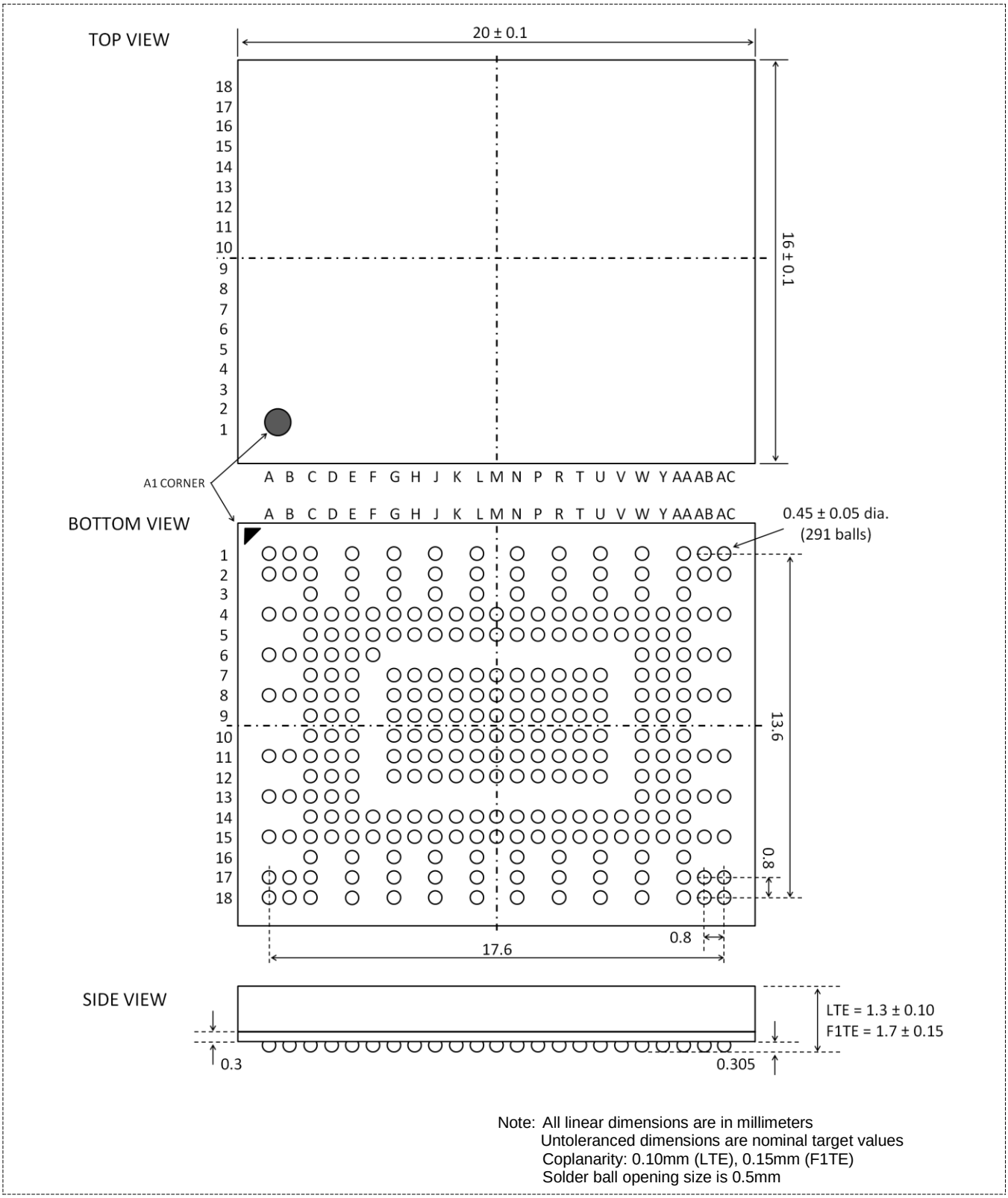


Figure 3-2: NVMe NANDrive 291-Ball, Ball Grid Array (BGA)

Revision History

Number	Description	Date
00.100	Initial Release as Advance Factsheet	February 29, 2024

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